TECHNICAL WHITEPAPER

# Industrial 8Gb DDR4 DRAM Chip

High-speed DDR4 up to 3200 MT/s with CA parity, write CRC, and PPR support, screened for industrial and extended temperature grades up to 105°C.

| JEDEC Compliant | Industrial & Extended Temp<br>−40°C to 85°C & −55°C to 105°C | 8GB |
|---|---|---|

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# 1. Executive Summary

Ningbo Loongtion Intelligent Technology Co., Ltd. (Loongtion®) presents the Loongtion 8Gb DDR4 DRAM chip, a JEDEC-compliant high-speed dynamic random access memory solution engineered for demanding industrial, embedded, medical, and commercial applications. This product delivers a per-die density of 8Gb in x8 (1G × 8) and x16 (512M × 16) configurations, supporting transfer rates up to DDR4-3200 (3200 MT/s).

Key differentiators include wide industrial temperature range options spanning –40°C to +85°C and an extended range of –55°C to +105°C, robust reliability features such as Command/Address (CA) parity, write CRC, on-die termination (ODT), and Post-Package Repair (PPR) support. Advanced power management through Max Power Saving Mode and Fine Granularity Refresh (FGR) enables efficient operation across varied thermal environments.

The Loongtion 8Gb DDR4 DRAM chip is well-suited for target markets including industrial automation, embedded systems, medical devices, networking and telecommunications infrastructure, and commercial computing platforms requiring high reliability, long lifecycle support, and JEDEC-standard electrical and timing compliance.

*Note: Specific module-level capacities (e.g., 8GB as a single- or multi-die product) are not detailed in source documentation; the documented density per DRAM die is 8Gb.*

# 2. Product Overview

The Loongtion 8Gb DDR4 DRAM chip is a high-speed, double-data-rate synchronous DRAM designed in accordance with the JEDEC Standard No. 79-4 for DDR4 SDRAM. The product is available in two die configurations: x8 (1G × 8) and x16 (512M × 16), supporting a maximum data transfer rate of 3200 MT/s. The device operates from a nominal power supply of 1.2 V (VDD = VDDQ) with a separate 2.5 V VPP supply.

## 2.1 Part Numbers

| Part Number | Configuration | Package | Temperature Range |
|---|---|---|---|
| YZ48G08V-F7HPI-M(0) | 8Gb, 1G × 8 | 78-ball FBGA | –40°C to +85°C |
| YZ48G08V-F7HPI-M | 8Gb, 1G × 8 | 78-ball FBGA | –55°C to +105°C |
| YZ48G16V-F9HPI-M(0) | 8Gb, 512M × 16 | 96-ball FBGA | –40°C to +85°C |
| YZ48G16V-F9HPI-M | 8Gb, 512M × 16 | 96-ball FBGA | –55°C to +105°C |

## 2.2 Document Revision History

| Revision | Date | Description |
|---|---|---|
| Rev 1.0 | 2023/05 | Initial Draft |
| Rev 1.1 | 2023/06 | Official Release |
| Rev 1.2 | 2025/03 | Updated Dimensions |
| Rev 1.3 | 2025/10 | Updated Reset and Initialization Description |

## 3. Technology and Architecture

The Loongtion 8Gb DDR4 DRAM chip is built upon the JEDEC DDR4 architecture, incorporating an 8n prefetch design, advanced bank organization, and a comprehensive set of programmable mode registers to support flexible system integration.

### 3.1 8n Prefetch Architecture

A single read or write operation consists of a single 8n-bit-wide, 4-clock-cycle data transfer at the internal DRAM core, followed by eight corresponding n-bit-wide, 4-clock-cycle data transfers at the I/O pins. This prefetch architecture enables the double-data-rate interface to achieve high throughput while maintaining core operating efficiency.

### 3.2 Bank Organization

| Configuration | Total Banks | Bank Groups | Banks per Group |
|---|---|---|---|
| x8 (1G × 8) | 8 | 4 (BG0–BG1) | 2 (BA0–BA1) |
| x16 (512M × 16) | 4 | 2 (BG0 only) | 2 (BA0–BA1) |

### 3.3 Address Mapping

| Parameter | ×8 Configuration | ×16 Configuration |
|---|---|---|
| Row address | A0–A15 | A0–A15 |
| Column address | A0–A9 | A0–A9 |
| Page size | 1 KB | 2 KB |

Address bits registered coincident with the ACTIVATE command select the bank group (BG0–BG1 in x8; BG0 in x16), bank (BA0–BA1), and row address (A0–A17). Address bits registered coincident with a Read or Write command select the starting column address, auto precharge (via A10), and burst chop/mode selection (via A12).

### 3.4 Clock and Strobe Architecture

All control and address inputs are synchronized with a pair of externally provided differential clocks (CK_t, CK_c). Inputs are latched at the crossing point of the differential clock (both CK rising and CK falling). All I/Os are source-synchronized with a pair of bidirectional differential data strobes (DQS_t, DQS_c). The interface transfers two data words per clock cycle at the I/O pins (double data rate).

On-chip PLL ensures CK-to-DQ and CK-to-DQS timing alignment.

### 3.5 Burst Architecture

- **Burst length options:** Burst Length 8 (BL8) fixed via MRS, or Burst Chop 4 (BC4) fixed via MRS, or BL8/BC4 selectable on-the-fly via A12.
- **Read burst type:** Sequential or Interleave (selectable via MR0 A3).

### 3.6 Mode Register Architecture

The device uses eight mode registers (MR0–MR7) and one RCW register, selected via address bits A2:A0. Key mode register functions include:

| Register | Key Functions |
|---|---|
| MR0 | Write Recovery (WR), Read Precharge (RTP), CAS Latency (CL), Burst Length OTF mode, read burst type |
| MR1 | RTT_NOM, Output Driver Impedance Control |
| MR2 | RTT_WR, CWL (CAS Write Latency), CRC error handling |
| MR3 | Fine Granularity Refresh Mode, CRC/DM timing, MPR data format, Temperature Sensor, PDA mode control |
| MR4 | Maximum Power-Down mode, CS to CMD/ADDR Delay Mode |
| MR5 | RTT_PARK, C/A Parity Latency Mode |
| MR6 | tCCD_L, tDLLK, VrefDQ Training |
| MR7 | Ignored by DRAM |

### 3.7 Multi-Purpose Register (MPR)

| Page | Function |
|---|---|
| Page 0 | Training Mode |
| Page 1 | CA Parity Error Log |
| Page 2 | MRS Readout (includes temperature sensor status bits A4:A3) |
| Page 3 | Supplier use only |

MPR default values: MPR0 = 0x55 (01010101), MPR1 = 0x33 (00110011), MPR2 = 0x0F (00001111), MPR3 = 0x00 (00000000).

## 4. Key Features and Differentiators

### 4.1 Wide Temperature Range Options

The Loongtion 8Gb DDR4 DRAM chip is available in two temperature grades:

- **Industrial range:** –40°C to +85°C
- **Extended industrial range:** –55°C to +105°C

This differentiates the product from commercial-only DDR4 solutions and makes it suitable for harsh-environment applications.

### 4.2 Command/Address (CA) Parity

CA parity is supported via the MR5 register, providing command/address bus error detection. CA parity latency mode is configurable. Even parity is used.

### 4.3 Write CRC

Cyclic Redundancy Check (CRC) on the data bus is supported for write operations, enabling detection of data corruption during transmission.

## 4.4 Data Bus Inversion (DBI)

DBI reduces power consumption and switching noise by inverting data when the majority of bits in a byte are High.

## 4.5 On-Die Termination (ODT)

Full ODT support includes RTT_NOM, RTT_WR, and RTT_PARK with multiple programmable impedance values:

| Parameter | Supported Values |
|---|---|
| RTT_NOM | Disabled, RZQ/4, RZQ/2, RZQ/6, RZQ/1, RZQ/5, RZQ/3, RZQ/7 |
| RTT_WR | Dynamic ODT Off, RZQ/2, RZQ/1, Hi-Z, RZQ/3 |
| RTT_PARK | Disabled, RZQ/4, RZQ/2, RZQ/6, RZQ/1, RZQ/5, RZQ/3, RZQ/7 |

Dynamic ODT is supported via RTT_WR.

## 4.6 Write Leveling

Write leveling is supported to compensate for clock-to-strobe skew inherent in fly-by topology. The memory controller must have adjustable delay on DQS_t–DQS_c to align the rising edge with the clock at the DRAM pins. On x16 devices, the two byte lanes are leveled independently: high data bits provide feedback on UDQS, low data bits on LDQS.

## 4.7 Post-Package Repair (PPR)

Hard PPR (MR4 A[13]) and Soft PPR (MR4 A[5]) modes are supported. PPR is supported in x16 configuration only and requires a Precharge All command.

## 4.8 Fine Granularity Refresh (FGR)

Refresh rate options include:

- Normal (Fixed 1×)
- Fixed 2×
- Fixed 4×
- Enable on-the-fly 2×
- Enable on-the-fly 4×

## 4.9 Temperature Sensor Readout

The internal temperature sensor provides readout updated within 32 ms when MR3 bit A5=1. The sensor is disabled when A5=0.

## 4.10 Additional Features

- Asynchronous reset (RESET_n pin)
- ZQ calibration (240 Ω reference resistor)
- Per DRAM Addressability (PDA)
- Internal Vref Monitor

- VrefDQ Training (two ranges: Range 1 and Range 2)
- Read Preamble Training Mode
- Self-Refresh Termination
- Max Power Saving Mode (MR4 A[1])
- DLL-off mode
- Low-power self-refresh
- Connectivity test mode (TEN pin required on x16 devices, not supported on x4/x8)
- Temperature Controlled Refresh (TCR) with Normal and Extended ranges

# 5. Technical Specifications

## 5.1 Power Supply Rails

| Parameter | Nominal | Min | Max |
|---|---|---|---|
| VDD = VDDQ | 1.2 V | 1.14 V | 1.26 V |
| VPP | 2.5 V | 2.375 V | 2.75 V |
| VrefCA | VDD/2 | 0.49 × VDD | 0.51 × VDD |
| VSS | Ground | — | — |
| VSSQ | DQ Ground | — | — |

## 5.2 Absolute Maximum Ratings

| Parameter | Min | Max |
|---|---|---|
| VDD relative to VSS | –0.3 V | 1.5 V |
| VDDQ relative to VSS | –0.3 V | 1.5 V |
| VPP relative to VSS | –0.3 V | 3.0 V |
| Voltage on any pin (except VREFCA) relative to VSS | –0.3 V | 1.5 V |

## 5.3 ESD and Latch-Up Ratings

| Parameter | Value |
|---|---|
| ESD Rating (HBM) | 2 kV |
| ESD Rating (CDM) | 500 V |
| Latch-up (ILU) | >100 mA, 1.5 × VDDmax |
| Maximum Rate of Change of External Ambient Temperature (EETCRMax) | 15°C/min |

## 5.4 Package Options

| Configuration | Package Type | Ball Count |
|---|---|---|
| x8 | JEDEC standard FBGA | 78-ball |
| x16 | JEDEC standard FBGA | 96-ball |

## 5.5 78-ball FBGA (×8 Configuration) Dimensions

| Parameter | Nominal | Min | Max |
|---|---|---|---|

| Package body (D) | 9.00 mm | 8.90 mm | 9.10 mm |
|---|---|---|---|
| Package body (E) | 14.00 mm | 13.90 mm | 14.10 mm |
| Ball pitch (d) | 0.80 mm | — | — |
| Ball diameter (b) | 0.47 mm | 0.42 mm | 0.52 mm |
| Package height (A) | 1.12 mm | — | 1.20 mm |
| Standoff (A1) | 0.78 mm | 0.73 mm | 0.83 mm |
| Mold thickness (A2) | 0.34 mm | 0.30 mm | 0.38 mm |

### 5.6 96-ball FBGA (×16 Configuration) Dimensions

| **Parameter** | **Nominal** | **Min** | **Max** |
|---|---|---|---|
| Package body (D) | 9.00 mm | 8.90 mm | 9.10 mm |
| Package body (E) | 14.00 mm | 13.90 mm | 14.10 mm |
| Ball pitch (d) | 0.80 mm | — | — |
| Ball diameter (b) | 0.47 mm | 0.42 mm | 0.52 mm |
| Package height (A) | 1.12 mm | — | 1.20 mm |
| Standoff (A1) | 0.78 mm | 0.73 mm | 0.83 mm |
| Mold thickness (A2) | 0.34 mm | 0.30 mm | 0.38 mm |

### 5.7 I/O Pin Package Parameters

| **Parameter** | **1G × 8 (DDR4-2400/2666)** | **1G × 8 (DDR4-2933/3200)** | **512M × 16** |
|---|---|---|---|
| ZIO (Ω) | 45 to 85 | 45 to 85 | 45 to 85 |
| TdIO (ps) | 14 to 42 | 14 to 40 | 14 to 45 |
| LIO (nH) | up to 3.3 | up to 3.3 | up to 3.4 |
| CIO (pF) | up to 0.78 | up to 0.78 | up to 0.82 |

### 5.8 DQS Pin Package Parameters

| **Parameter** | **1G × 8 (DDR4-2400/2666)** | **1G × 8 (DDR4-2933/3200)** | **512M × 16** |
|---|---|---|---|
| ZIO_DQS (Ω) | 45 to 85 | 45 to 85 | 45 to 85 |
| TdIO_DQS (ps) | 14 to 42 | 14 to 40 | 14 to 45 |
| LIO_DQS (nH) | up to 3.3 | up to 3.3 | up to 3.4 |
| CIO_DQS (pF) | up to 0.78 | up to 0.78 | up to 0.82 |

Delta Zpkg for DQS_t and DQS_c: up to 10 Ω. Delta delay for DQS_t and DQS_c: up to 5 ps.

### 5.9 CTRL Pin Package Parameters

| **Parameter** | **Value** |
|---|---|
| ZI_CTRL | 50 to 90 Ω |
| TDI_CTRL | 14 to 42 ps |
| LI_CTRL | up to 3.4 nH |
| CI_CTRL | up to 0.7 pF |

### 5.10 CMD/ADD Pin Package Parameters

| **Parameter** | **1G × 8 (DDR4-2400/2666)** | **1G × 8 (DDR4-2933/3200)** | **512M × 16** |
|---|---|---|---|
| ZIADD_CTRL (Ω) | 50 to 90 | 50 to 90 | 50 to 90 |

| TdIADD_CTRL (ps) | 14 to 45 | 14 to 40 | 14 to 52 |
|---|---|---|---|
| LIADD_CTRL (nH) | up to 3.6 | up to 3.6 | up to 3.9 |
| CIADD_CTRL (pF) | up to 0.74 | up to 0.74 | up to 0.86 |

## 5.11 Clock Pin Package Parameters

| Parameter | Value |
|---|---|
| ZCK | 50 to 90 Ω |
| TDCK | 14 to 42 ps |
| LI_CK | up to 3.4 nH |
| CI_CK | up to 0.7 pF |
| Delta Zpkg for CLK_t and CLK_c | up to 10 Ω |
| Delta Delay for CLK_t and CLK_c | up to 5 ps |

## 5.12 Other Pin Package Parameters

| Pin | ZO (Ω) | TdO (ps) |
|---|---|---|
| ZQ | up to 100 | 20 to 90 |
| ALERT | 40 to 100 | 20 to 55 |

## 5.13 Output Driver Impedance

The output driver supports two programmable impedance settings referenced to RZQ = 240 Ω.

### RZQ/7 = 34 Ω Setting

| Condition | RON34Pd (min/nom/max) | RON34Pu (min/nom/max) |
|---|---|---|
| VOLdc = 0.5 × VDDQ | 0.8 / 1.0 / 1.1 | 0.9 / 1.0 / 1.25 |
| VOMdc = 0.8 × VDDQ | 0.9 / 1.0 / 1.1 | 0.9 / 1.0 / 1.1 |
| VOHdc = 1.1 × VDDQ | 0.9 / 1.0 / 1.25 | 0.8 / 1.0 / 1.1 |

### RZQ/5 = 48 Ω Setting

| Condition | RON48Pd (min/nom/max) | RON48Pu (min/nom/max) |
|---|---|---|
| VOLdc = 0.5 × VDDQ | 0.8 / 1.0 / 1.1 | 0.9 / 1.0 / 1.25 |
| VOMdc = 0.8 × VDDQ | 0.9 / 1.0 / 1.1 | 0.9 / 1.0 / 1.1 |
| VOHdc = 1.1 × VDDQ | 0.9 / 1.0 / 1.25 | 0.8 / 1.0 / 1.1 |

## 5.14 Supported Latency Values

| Parameter | Supported Values |
|---|---|
| CAS Latency (CL) | 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 26, 28, 30, 32 |
| CAS Write Latency (CWL) | 9, 10, 11, 12, 14, 16, 18, 20 |
| Additive Latency (AL) | 0, CL–1, CL–2 |
| Write Recovery (WR) | 10, 12, 14, 16, 18, 20, 22, 24, 26 |
| Read to Precharge (RTP) | 5, 6, 7, 8, 9, 10, 11, 12, 13 |

*Note: Specific timing parameters (tCK min, tRCD, tRP, etc.) for speed bin operation are not specified in source documentation; refer to the JEDEC DDR4 standard for respective speed bin limits. Additive Latency CL–2 may be reserved for some configurations.*

### 5.15 Environmental Compliance

| Parameter | Value |
|---|---|
| Lead-free and RoHS compliance | Compliant |
| Moisture Sensitivity Level (MSL) | 3 |
| Maximum PCB Assembly Reflow Cycles | 3 |
| Weight | 0.248 g |
| Lifetime | 10 years |

## 6. Performance and Reliability

### 6.1 Data Transfer Rate

The Loongtion 8Gb DDR4 DRAM chip supports a maximum transfer rate of DDR4-3200 (3200 MT/s), with speed bins supporting 2400, 2666, and 2933 MT/s as documented in package parameter tables.

### 6.2 Power-Up Characteristics

| Parameter | Min | Max |
|---|---|---|
| VDD slew rate (VDD_sla) | 0.004 V/ms | 600 V/ms |
| VDD ramp time (VDD_ona) | TBD | 200 ms |
| Power supply module capability | 180 mA within 400 ns | — |

### 6.3 Temperature Reliability

- Maximum rate of change of external ambient temperature: 15°C/min.
- Product lifetime: 10 years as specified in source documentation.
- Temperature-Controlled Refresh (TCR) with Normal and Extended ranges supports reliable operation across the full temperature spectrum.

### 6.4 Error Detection and Robustness

- **CA Parity** enables detection of command/address bus errors.
- **Write CRC** provides data bus error detection for write operations.
- **Hard and Soft Post-Package Repair (PPR)** allows repair of defective memory cells after packaging (x16 configuration only).
- **On-die termination** reduces signal reflections and improves signal integrity across the memory bus.
- **ESD robustness:** 2 kV HBM, 500 V CDM.
- **Latch-up immunity:** >100 mA, 1.5 × VDDmax.

### 6.5 Refresh Management

Fine Granularity Refresh (FGR) allows the system to adjust refresh rates in response to operating temperature, reducing refresh overhead at lower temperatures and ensuring data retention at elevated

temperatures. Self-Refresh with programmable termination further enhances low-power standby operation.

*Note: TBW (Terabytes Written) is not applicable to DRAM and is not specified in source documentation.*

## 7. Applications and Target Markets

### 7.1 Industrial Automation

The wide temperature range options (–40°C to +85°C and –55°C to +105°C) make the Loongtion 8Gb DDR4 DRAM chip suitable for factory automation, programmable logic controllers (PLCs), robotics, and test and measurement equipment operating in unconditioned environments.

### 7.2 Embedded Systems

DDR4 DRAM chips are well-suited for single-board computers, IoT gateways, edge servers, and networking equipment (routers, switches, network appliances) requiring JEDEC-compliant memory with advanced features.

### 7.3 Medical Devices

Medical imaging systems, patient monitors, and diagnostic equipment benefit from the product's high reliability, long lifecycle support (10-year lifetime), and robust error detection features.

### 7.4 Commercial Computing

Servers, storage systems, workstations, and high-performance computing platforms can leverage the 3200 MT/s transfer rate, ECC features (via CA parity and CRC), and flexible ODT configuration.

### 7.5 Telecommunications

Base stations, optical transport equipment, and network appliances require the low latency, high reliability, and wide temperature operation that this DDR4 solution provides.

## 8. System Integration and Design Considerations

### 8.1 Power Supply Sequencing

- VDD and VDDQ must always be within 300 mV of each other. Under all conditions, VDDQ must be ≤ VDD.
- VDD and VDDQ can be applied in either order (VDD before or same time as VDDQ, without slope reversal).
- VPP must ramp simultaneously with or earlier than VDD, and VPP must always be equal to or ≥ VDD/VDDQ.
- VDDQ before or same time as VTT and VrefCA, without slope reversal.
- VPP before or same time as VDD, without slope reversal.
- Rise time of power supply voltage from 300 mV to VDD min must not exceed 200 ms.

- VDD slew rate measured between 300 mV and 80% VDD, bandwidth limited to 20 MHz.

## 8.2 Reset and Initialization

- During power-up, RESET_n and TEN must be kept below 0.2 × VDD.
- After power supply stabilizes, RESET_n must be kept below 0.2 × VDD for at least 200 µs.
- After power supply stabilizes, TEN (x16 configuration) must be kept below 0.2 × VDD for at least 700 µs.

## 8.3 VREF Configuration

VREF must be configured in a three-step procedure:

1. Configure A7 and A6 simultaneously.
2. A5:A0 set the Vref-DQ value.
3. Set A7 = 0.

Configuring VREF in a single step may cause errors.

## 8.4 Write Leveling for Fly-By Topology

Write leveling is required for systems using fly-by topology for the command/address bus. The memory controller must adjust the delay on DQS_t–DQS_c to align the rising edge with the clock at the DRAM pins. During leveling:

- DQS_t–DQS_c is driven by the controller and must be terminated according to the rank populated in the DRAM.
- DQ bus driven by the DRAM must be terminated at the controller.
- All data bits should pass level feedback to the controller in DRAM configurations x8 and x16.
- On x16 devices, high and low byte lanes should be leveled independently: high data bits provide feedback on UDQS, low data bits on LDQS.

## 8.5 ODT Configuration Guidelines

- Use RTT_NOM for idle states.
- Use RTT_WR (Dynamic ODT) during write operations to match the characteristic impedance of the memory bus.
- Use RTT_PARK for parked memory ranks.
- Dynamic ODT can be enabled or disabled based on system requirements.

## 8.6 Signal Integrity Considerations

- Package parasitic tables for I/O, DQS, CTRL, CMD/ADD, clock, and other pins are provided in Section 5 for simulation use.
- Overshoot/undershoot limits are defined per pin type and speed grade in the source documentation; these must be observed to maintain signal integrity. Limits vary between DDR4-2400, 2666, 2933, and 3200 speed bins.

- Differential pairs (CK_t/CK_c, DQS_t/DQS_c) require tight impedance matching: delta Zpkg ≤ 10 Ω; delta delay ≤ 5 ps.
- Package electrical specifications apply only to single-die devices; stacked/dual-die devices are not included in the documented parameters.

### 8.7 PCB Layout Recommendations

- Fly-by topology is recommended for address/command/control routing to minimize stub effects.
- On-die termination eliminates the need for external termination resistors.
- Follow JEDEC DDR4 design guidelines for trace length matching, via count minimization, and decoupling capacitor placement.

### 8.8 Thermal Management

- Package height up to 1.20 mm should be considered when designing thermal solutions for extended temperature range parts.
- The internal temperature sensor provides real-time die temperature readout, enabling dynamic refresh rate control via FGR.

## 9. Standards Compliance and Quality

The Loongtion 8Gb DDR4 DRAM chip is designed and manufactured in compliance with the following industry standards:

- **JEDEC DDR4 Standard (No. 79-4):** Full compliance with DDR4 electrical, timing, and protocol specifications.
- **RoHS Directive:** Lead-free and RoHS compliant.
- **Moisture Sensitivity Level (MSL):** Level 3 per IPC/JEDEC J-STD-020.
- **Maximum Reflow Cycles:** 3 cycles at peak temperature per JEDEC specifications.

The product supports all mandatory JEDEC DDR4 features including:

- DLL ON mode
- 1tCK and 2tCK switching modes
- ZQ calibration (initial and periodic)
- Asynchronous reset
- Low-power self-refresh
- Auto precharge capability
- Burst chop (BC4) and burst length 8 (BL8) modes
- Read/write training (including Vref training and write leveling)

Quality assurance is supported through documented electrical test parameters, package parasitic characterization, and environmental compliance verification.

## 10. Ordering Information

The following part numbers are available for the Loongtion 8Gb DDR4 DRAM chip:

| Part Number | Configuration | Package | Temperature Range |
|---|---|---|---|
| YZ48G08V-F7HPI-M(0) | 8Gb, 1G × 8 | 78-ball FBGA | –40°C to +85°C |
| YZ48G08V-F7HPI-M | 8Gb, 1G × 8 | 78-ball FBGA | –55°C to +105°C |
| YZ48G16V-F9HPI-M(0) | 8Gb, 512M × 16 | 96-ball FBGA | –40°C to +85°C |
| YZ48G16V-F9HPI-M | 8Gb, 512M × 16 | 96-ball FBGA | –55°C to +105°C |

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*Note: Additional part numbers, custom configurations, or tray/reel packaging options not listed in source documentation should be confirmed directly with Loongtion.*

## 11. About Loongtion

Ningbo Loongtion Intelligent Technology Co., Ltd. (Loongtion®) is a China-based developer and supplier of memory and solid-state storage products for industrial, embedded, medical, and commercial applications. The company's product portfolio includes DDR3, DDR4, DDR5, and LPDDR4X DRAM chips, eMMC 5.1, M.2 NVMe SSD, and NVMe BGA SSD solutions. Loongtion serves a global customer base with high-performance, reliable memory and storage solutions designed to meet the rigorous demands of mission-critical systems across multiple industries.

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## Disclaimer

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